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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,705	03/02/2000	Chunlin Liang	042390.P5771D	4202

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02/27/2003

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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/517,705

Applicant(s)

LIANG ET AL. PS

Examiner

Steven Loke

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,16 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,16 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 15.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 16 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Dash et al.

In regards to claim 1, Dash et al. show all the elements of the claimed invention in fig. 9. It is a circuit device comprising: a first transistor (NMOS) including a first metal gate electrode (a portion of layer [56] formed above the channel region [52]) made of aluminum over a first gate dielectric [14'] on a first area (p-type region [52]) of a semiconductor substrate and having a work function (4.1 eV) corresponding to the work function of the N-type silicon; and a second transistor (PMOS) complementary to the first transistor including a second metal gate electrode [50] made of platinum silicide over a second gate dielectric [14''] on a second different area (n-type region [54]) of a semiconductor substrate and having a work function (5.7 eV) corresponding to the work function of the P-type silicon; and wherein the first metal gate electrode (a portion of layer [56] formed above the channel region [52]) and the second metal gate electrode [50] are not in direct physical contact with each other and are each separately disposed in respective ones of the first area (p-type region [52]) and the second area (n-type region [54]) of the semiconductor substrate.

In regards to claim 2, Dash et al. disclose the first metal gate electrode [56] (aluminum) is a pure metal.

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In regards to claim 16, Dash et al. disclose the first gate dielectric [14'] is silicon dioxide.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dash et al.

In regards to claim 17, Dash et al. differ from the claimed invention by not showing the first metal gate electrode is one of tantalum, tantalum nitride, molybdenum silicide, and molybdenum nitride. It would have been obvious for the first metal gate electrode is one of tantalum, tantalum nitride, molybdenum silicide, and molybdenum nitride since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

5. Applicant's arguments filed 1/27/03 have been fully considered but they are not persuasive.

It is urged, in page 2 of the remarks, that single structural element 56 performs two functions (e.g., gate electrode for N-channel transistor and a contact with gate electrode 50), does not render the single structural element into two structural elements.

However, it is important to note that a gate electrode is defined as an electrode layer formed above the channel region of a MOSFET and an electrode layer which connects the gate electrode of the MOSFET to the other region or electrode of another circuit

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element is considered as an interconnect electrode layer. Therefore, the middle portion of the electrode [56] which connects the gate electrode of the NMOSFET (a portion of layer [56] formed above the channel region [52]) and the gate electrode [50] of the PMOSFET is considered as the interconnect electrode layer. The single conductive layer [56] does show two structural elements, i.e., the first metal gate electrode and the interconnect electrode layer. The portion of layer [56] that is in direct contact with the gate electrode [50] is also considered as part of the interconnect electrode layer. The middle portion of the electrode layer [56] cannot be considered as a gate electrode because it is not formed above the channel region of the NMOSFET. Dash et al. meet the limitation of claims 1, 2 and 16 because the first metal gate electrode (a portion of layer [56] formed above the channel region [52]) and the second metal gate electrode [50] are not in direct physical contact with each other. The interconnect electrode layer (the middle portion of layer [56]) separates the first metal gate electrode (a portion of layer [56] formed above the channel region [52]) and the second gate electrode [50].

It is urged, in page 3 of the remarks, that claim 17 is not obvious over Dash et al. Since claim 17 depends from independent claim 1 and contains all of the limitations thereof, the same explanation set forth above regarding claim 1 also applies to claim 17. Therefore, claim 17 is still obvious over Dash et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
February 20, 2003

Steven Loh
Primary Examiner

